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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/569,799	02/27/2006	Kazuo Usui	XA10534	6470

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	**PAPER NUMBER**
2113	
MAIL DATE	**DELIVERY MODE**
08/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/569,799	USUI, KAZUO	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-18* is/are allowed.

6)☐ Claim(s) *1-3,6 and 8-11* is/are rejected.

7)☒ Claim(s) *4,5,7,12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/4/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 6, 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Debling U.S. Patent 6,973,592 in view of Microsoft Computer Dictionary (MCD).

As per claim 1, Debling teaches a microcomputer comprising: a central processing unit (column 3, line 20); a high-speed serial communication interface circuit which can be utilized for a debugging interface (column 3, lines 42-49); and an external bus interface circuit which can be connected to an external memory (column 5, lines 1-3), wherein the high-speed serial communication interface circuit has a plurality of ports therein and data can be mutually output from one of the ports in parallel with an input operation to the other port (column 4, lines 5-9), and the high-speed serial communication interface circuit receives a system program in the debugging mode and the system program thus received can be output from the external bus interface circuit together with a memory access control signal (column 5, lines 1-3, wherein an access signal would be needed when accessing the external memory). Debling doesn't explicitly teach wherein the plurality of ports comprises a buffer. MCD does teach a buffer (page 65). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to use the buffer of MCD in the system of Debling. One of ordinary skill in the art would have been motivated to use the buffer of MCD in the system of Debling because MCD teaches the buffer to be beneficial in the transmitting of data between two devices; an explicit need of Debling (column 3, lines 42-49).

As per claim 2, Debling teaches the microcomputer according to claim 1, wherein the high-speed serial communication interface circuit is a universal serial bus interface circuit (column 3, liens 42-49).

As per claim 3, Debling teaches the microcomputer according to claim 2, wherein further comprising capable of carrying out a control to transfer the received system program to a memory connected to the external bus interface (column 5, lines 1-3. Debling does not explicitly teach a DMA. MCD does teach a DMA (page 142). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the DMA of MCD in the process of Debling. One of ordinary skill in the art would have been motivated to use the DMA of MCD in the process of Debling because MCD teaches the DMA to be beneficial in the transfer of data between a memory and a connectd device; an explicit desire of Debling (column 4, line 63 – column 5, line 3).

As per claim 6, Debling teaches the microcomputer according to claim 1, further comprising a debugging dedicated low-speed serial communication interface circuit, the debugging dedicated low-speed serial communication interface circuit being usable for inputting control data to control the high-speed serial communication interface circuit in the debugging mode (column 2, lines 48-67).

As per claim 8, Debling teaches the microcomputer according to claim 6, wherein the debugging dedicated low-speed serial communication interface circuit is based on JTAG (column 2, lines 47-49). Debling does not explicitly teach a data register. MCD does teach a register (page 379). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a register of MCD in the process of Debling. One of ordinary skill in the art would have been motivated to use the register of MCD in the process of Debling because MCD teaches the register to be used to hold data for a particular purpose; an explicit need of Debling's JTAG function to hold test signals to be transferred (column 2, lines 42-57).

As per claim 9, Debling teaches the microcomputer according to claim 1, further comprising a trace control circuit, the trace control circuit successively storing, as trace information, an internal state obtained when the central processing unit executes the system program (column 1, lines 11-24; column 2, lines 66-67; wherein it is known to collect data from the target to be analyzed on the host which was sent back from the target. This monitoring is interpreted as tracing of the target).

As per claim 10, Debling teaches the microcomputer according to claim 9, wherein the high-speed serial communication interface circuit can be utilized for an external output of the trace information (column 4, lines 3-9).

As per claim 11, Debling teaches a method for developing a system program which is to be executed by a target device by using a host computer, an emulator and a target device, comprising: a first processing of storing a system program output through a high-speed serial communication by the host computer in one of two-plane buffers (buffers to ports see argument above) as a processing to be carried out by the emulator (column 3, lines 42-49); a second

processing of transmitting a system program stored in the other buffer (column 4, lines 29-31, wherein the JTAG can use the USB interface) to the target device through a low-speed serial communication in parallel with the first processing (column 3, lines 39-41. Debling does not teach a third processing of carrying out a handshake control of the low-speed serial communication together with the target device. MCD doe teach a handshake (page 212). It would have been obvious to one of ordinary skill at the time the invention was made to use a handshake of MCD in the process of Debling. One of ordinary skill in the art would have been motivated to use the handshake of MCD in the process of Debling because MCD teaches the handshake to be used to provide send and receive readiness between two devices; an explicit need of Debling (column 2, lines 48-57, wherein the host/target would need to have proper connection to enable the testing sequence).

Allowable Subject Matter

3. Claims 13-18 are allowed

4. Claims 4-5, 7, 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an examiner's statement of reasons for allowance: When read as a whole, claims 13 and 17 are allowable with respect to the following limitations:

With respect to claim 13, Debling does not teach, nor has desire of a debugging mode that is designated in a power-on reset, the central processing unit executes the first debugging control program to initialize the universal serial bus interface circuit to be operable, a second debugging control program is received by the universal serial bus interface circuit, the second debugging control program thus received is stored in the RAM, and a transition to an execution of the second debugging control program stored in the RAM is made.

With resepec to claim 17, Debling does not teach, nor have desire to in a power-on reset, the central processing unit executes the first debugging control program to initialize the universal serial bus interface circuit to be operable, a second debugging control program is received by the universal serial bus interface circuit, the second debugging control program thus received is stored in the buffer RAM, and the second debugging control program stored in the buffer RAM is output through the external interface circuit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

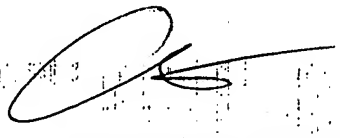
Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Christopher S. McCarthy
Examiner
Art Unit 2113